TOET20"+23+9260

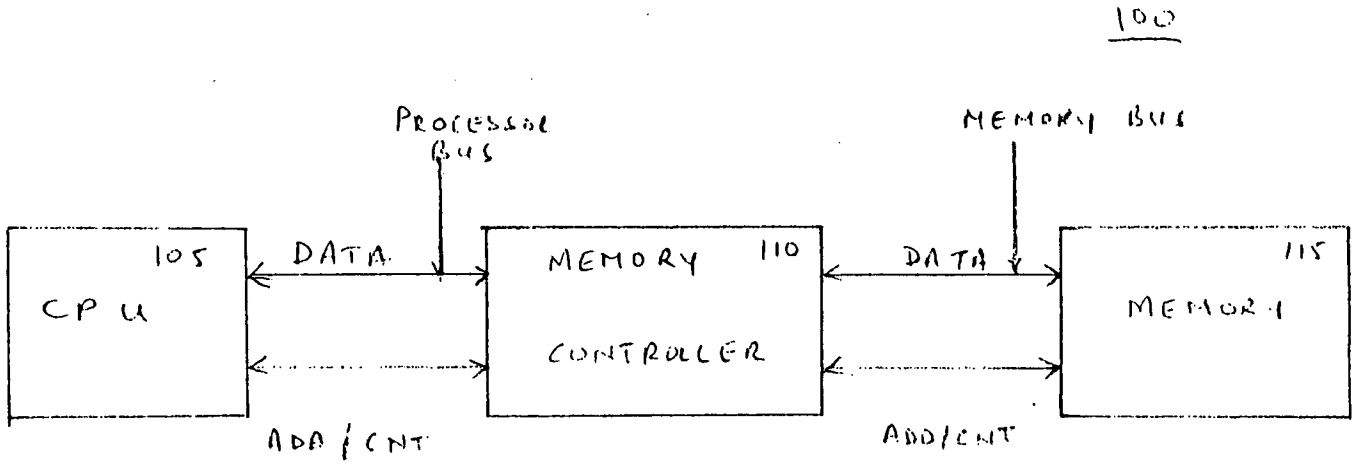

FIGURE 1

TOSTP20"+2424826

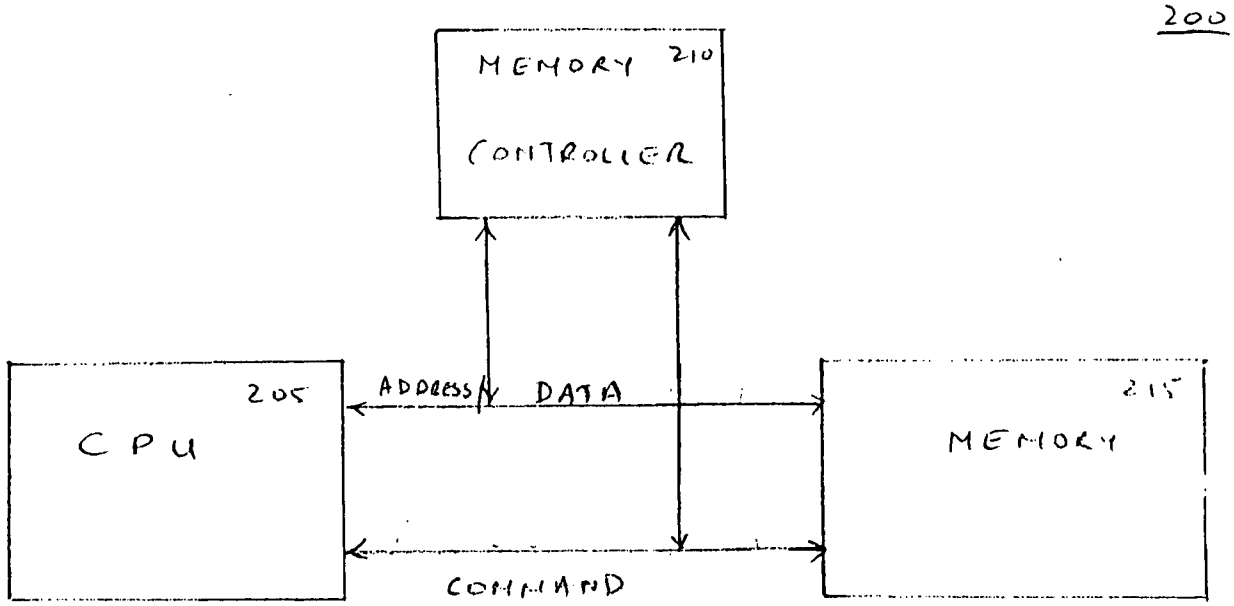

FIGURE 2

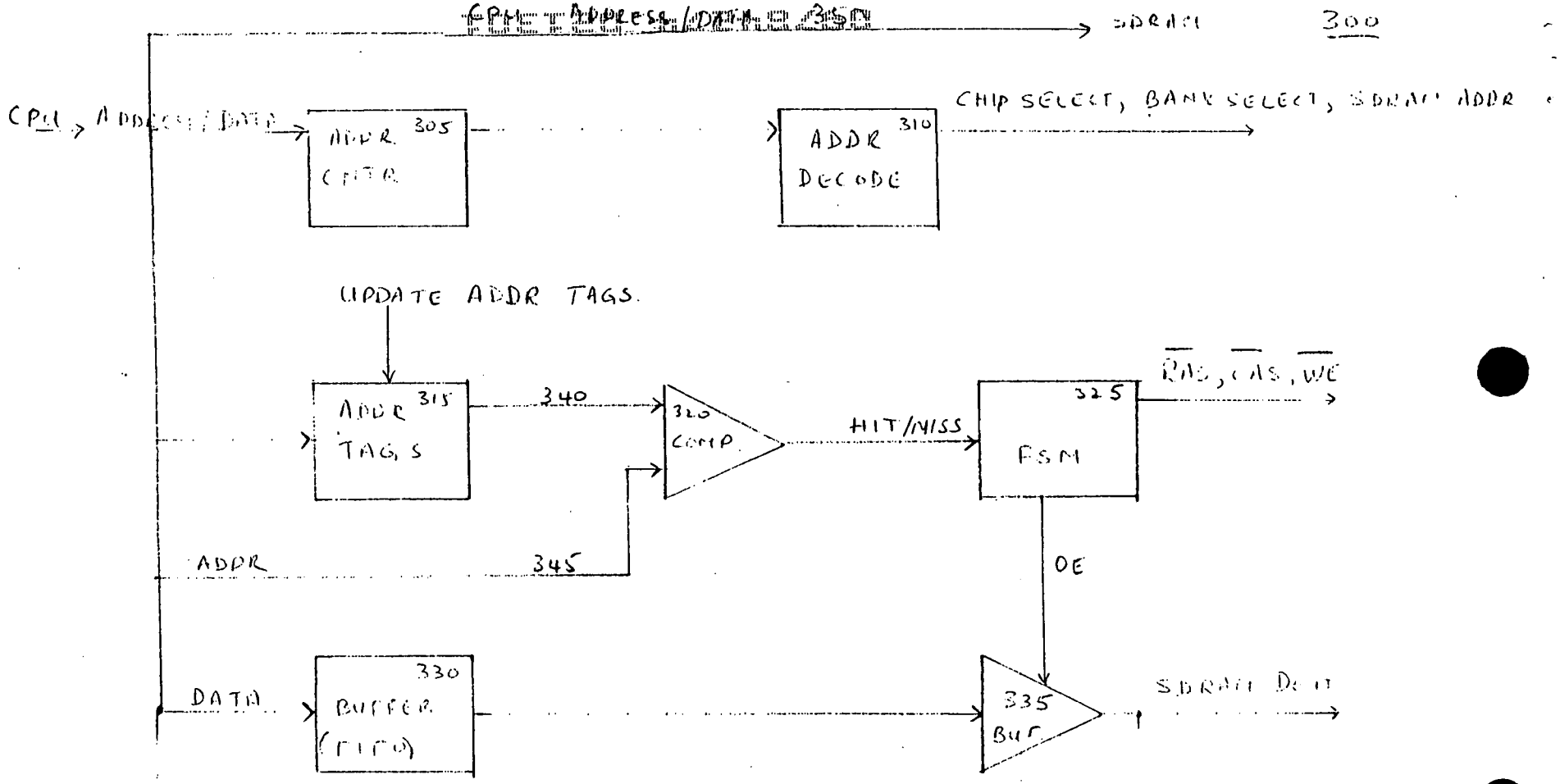
CPU Address/Data 350
SDRAM 300
CPU Address/Data
ADDR 305
CMP
ADDR 310
DECODE
CHIP SELECT, BANK SELECT, SDRAM ADDR
UPDATE ADDR TAGS
ADDR 315
TAGS
340
320
COMP
HIT/MISS
325
FSM
RAS, CAS, WE
ADDR
345
OE
DATA
330
BUFFER
(FIFO)
335
BUF
SDRAM DATA

FIGURE 3

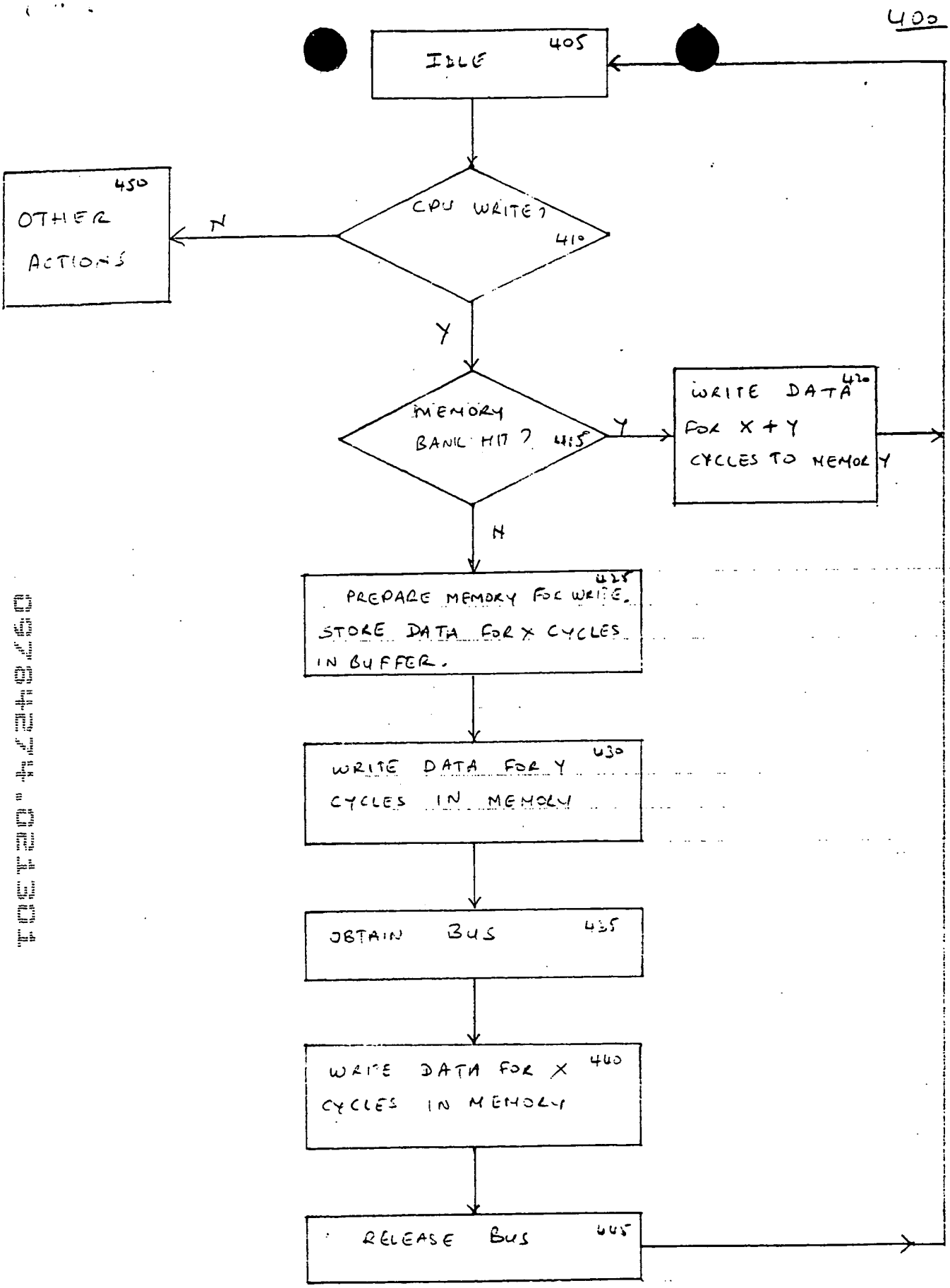
400
IDLE
405
CPU WRITE?
410
N
OTHER ACTIONS
450
Y
MEMORY BANK HIT?
415
Y
WRITE DATA FOR X+Y CYCLES TO MEMORY
420
N
PREPARE MEMORY FOR WRITE. STORE DATA FOR X CYCLES IN BUFFER.
425
WRITE DATA FOR Y CYCLES IN MEMORY
430
OBTAIN BUS
435
WRITE DATA FOR X CYCLES IN MEMORY
440
RELEASE BUS
445

FIGURE 4

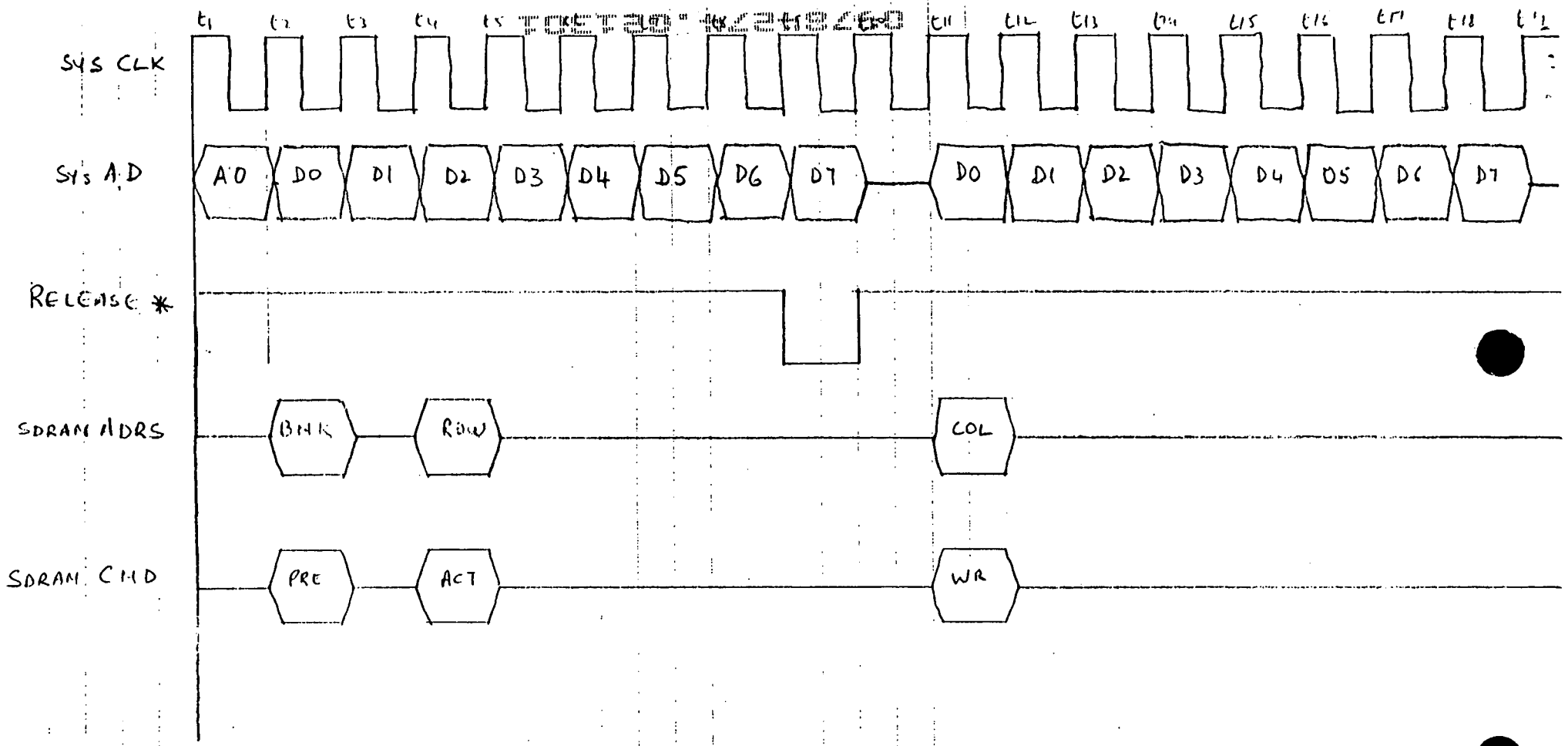

FIGURE 5 (PRIOR ART)

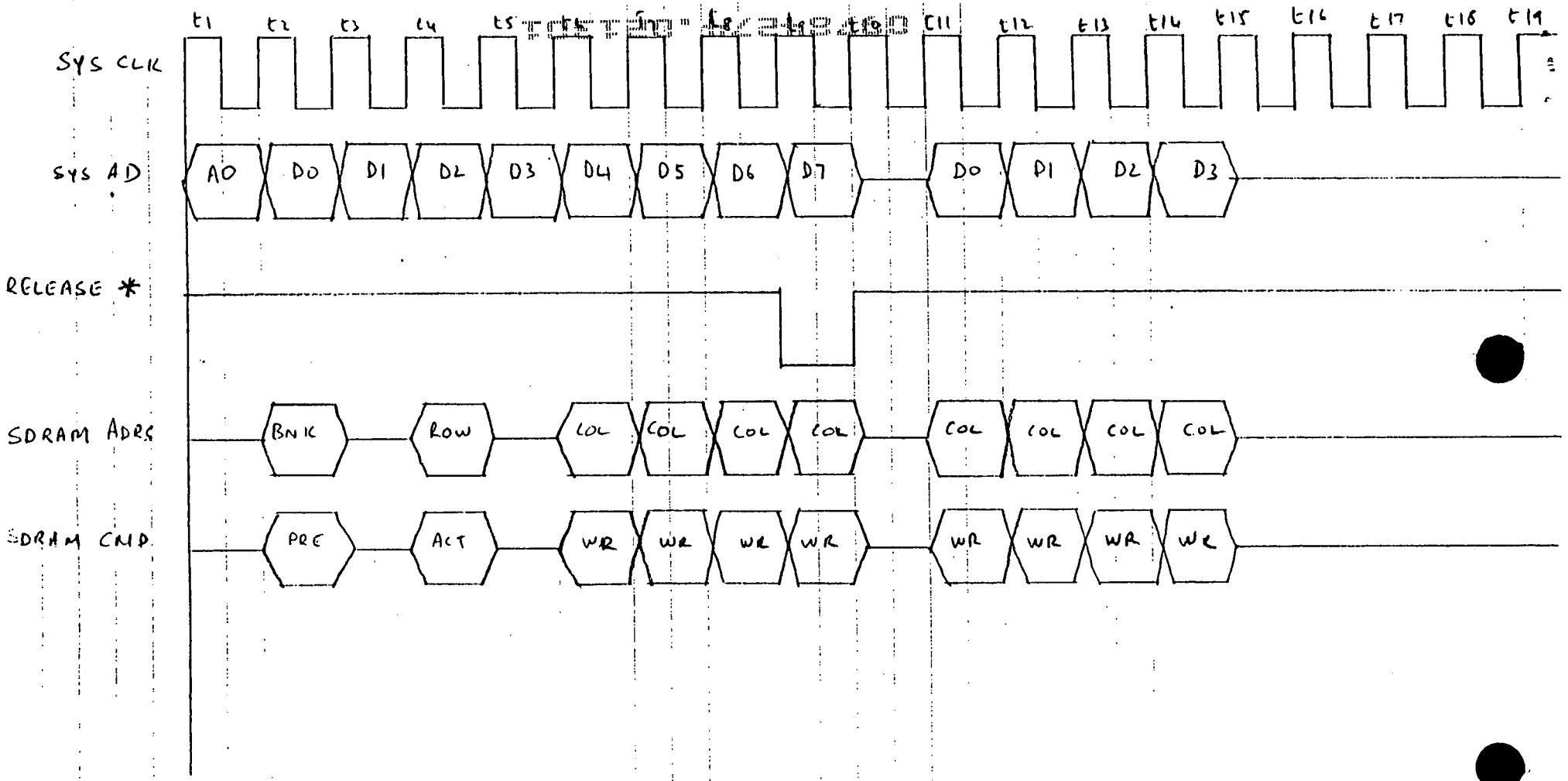
t1 t2 t3 t4 t5 t11 t12 t13 t14 t15 t16 t17 t18 t19
SYS CLK
SYS AD
A0 D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3
RELEASE *
SDRAM ADRS
BNK ROW COL COL COL COL COL COL COL COL
SDRAM CMD
PRE ACT WR WR WR WR WR WR WR WR

FIGURE 6

10E720 "42+8260

700

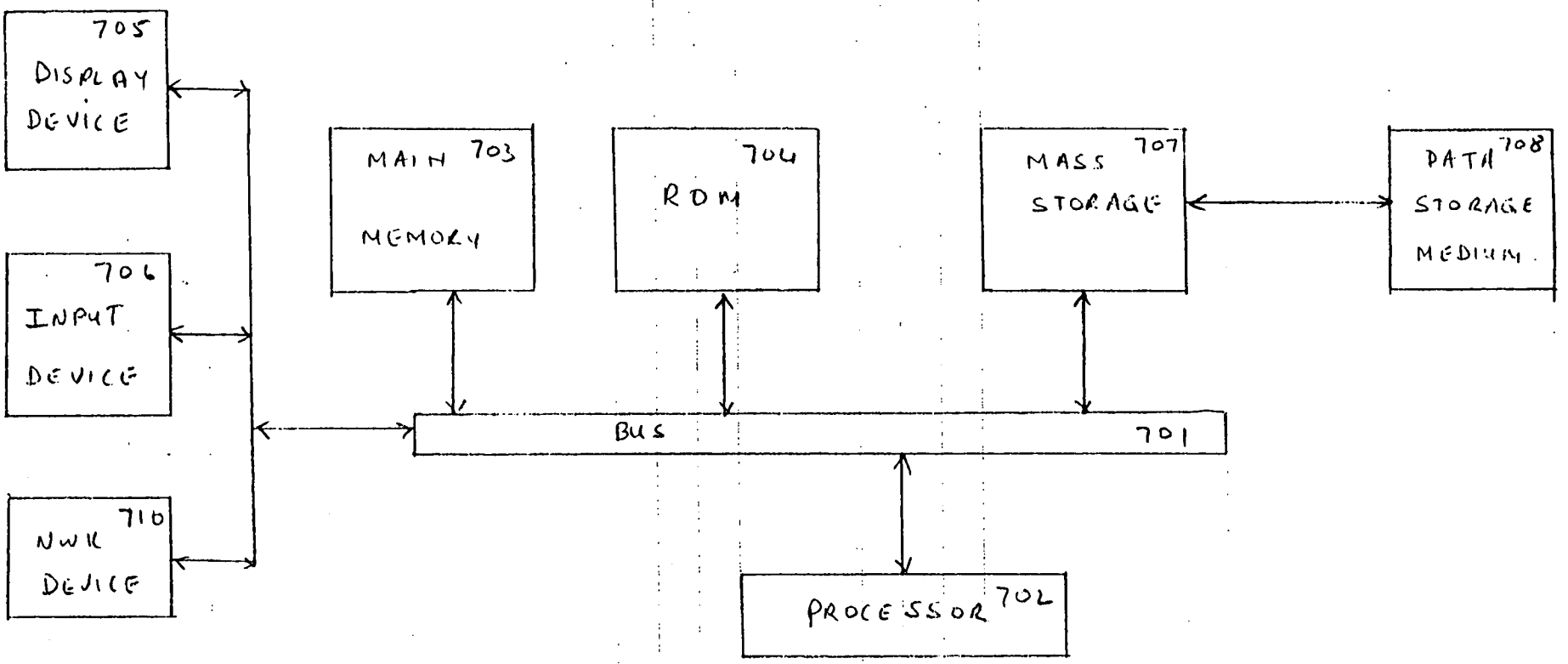

FIGURE 7